

NEC

NEC Corporation
Display Device Operations Unit
Color LCD Division

TFT COLOR LCD MODULE

Type: NL2432HC22-yyB
8.9cm (3.5 Type), QVGA

SPECIFICATIONS

(1st Edition, Issued on Nov.28, 2002)

PRELIMINARY

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1. DESCRIPTION

The NL2432CH22-yyB is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising an amorphous silicon TFT attached to each signal electrode, a driving circuit. This module is consist of LCD panel, Driver, Back light and Touch panel

The 8.9 cm (3.5 Type) diagonal display area contains 240×320 pixels and can display 262,144 colors simultaneously.

2. FEATURES

- Transflective type
- Back light and touch panel attached
- Recommended LCD controller: part no. S1L50282F23k100, NEC corp.
- High Brightness
- High contrast ratio
- Small footprint and light weight
- 6-bit digital RGB signals

3. APPLICATIONS

PDA's

4. STRUCTURE AND FUNCTION

Transflective TFT (thin film transistor) color LCD module is comprised of a TFT liquid crystal panel structure with LSIs for driving the TFT array. Sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate creates the TFT panel structure.

RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active-matrix addressing by the onboard signal processor and sent to the driver LSIs, which in turn addresses the individual TFT cells.

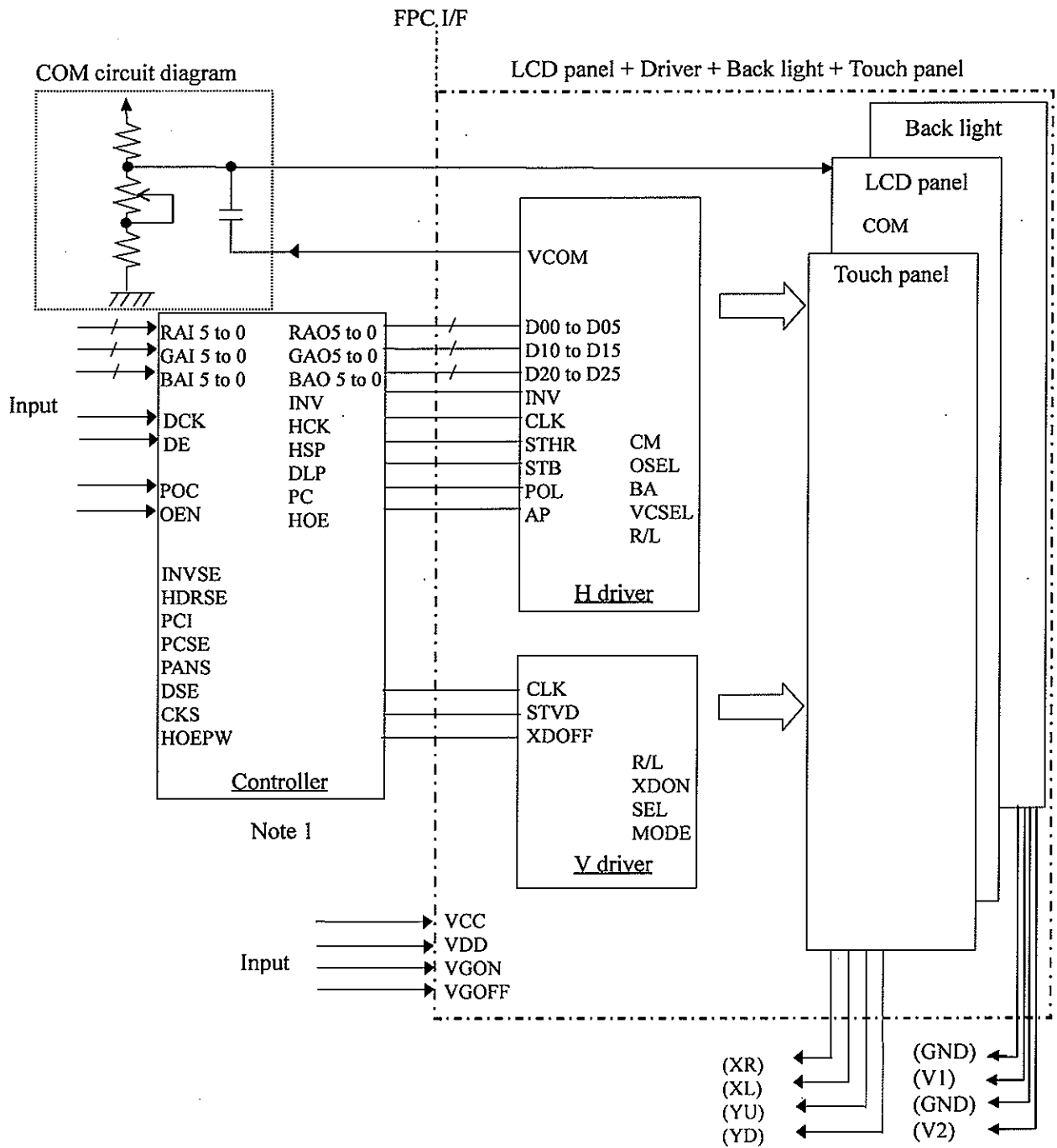
Acting as an Electro-optical switch, each TFT cell regulates light from the natural light and so on when activated by the data source. By regulating the amount of light reflection passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

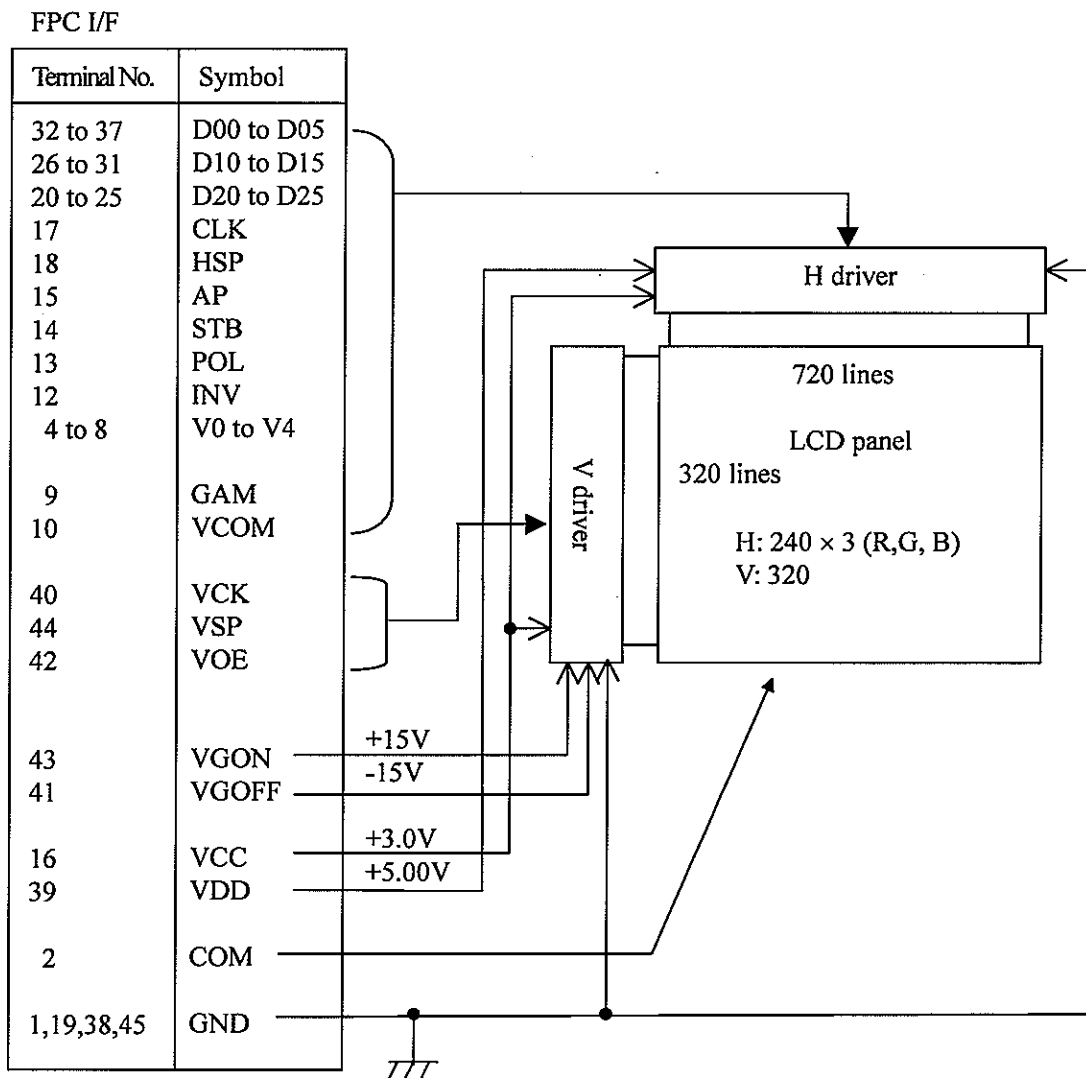
Display area	53.64 (H) × 71.52 (V) mm [Diagonal 8.9 cm]	
Drive system	a-Si TFT active matrix	
Display colors	262,144 colors	
Number of pixels	240 (H) × 320 (V)	
Pixel arrangement	RGB vertical stripe	
Pixel pitch	0.2235 (H) × 0.2235 (V) mm	
Module size	64.0 (Typ., H) × 85.0 (Typ., V) × (3.96) (Typ., D) mm [D: Not include FPC bending part]	
Weight	(37)g (Typ.)	
Luminance	TBD cd/m ² (Typ. At IL=18mA) (100)cd/m ² (Max. At IL=20mA)	
Contrast ratio	Reflective Mode	(10:1) (Typ.:With Touch panel)
	Transmittive Mode	TBD (Typ. At IL=18mA:With Touch panel) (100:1) (Typ. At IL=20mA:With Touch panel)
Reflection ratio	(7) % (Typ. With Touch panel)	
Signal system	Controller input (6-bit signals, DCK, DE, POC, OEN) signals Note 1	
Supply voltage	VCC 3.0 V (Typ. Logic) VDD 5.00 V (Typ. LCD H-driving) VGON 15.0 V (LCD V-driving) VGOFF -15.0 V (LCD V-driving)	
Power consumption	Panel	(19) mW (Typ.)
	Back light	(385)mW (Typ. At IL=18mA) (420)mW (Max.At IL=20mA)

Note 1: Refer to the controller (part no.: S1L50282F23k100) specifications.

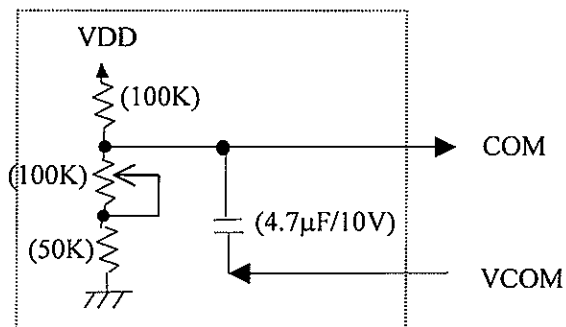
6. BLOCK DIAGRAM



Note 1 : Refer to the controller (part no.: S1L50282F23k100) specifications for input timings.



Reference design of COM circuit



7. GENERAL SPECIFICATIONS

Items	Specifications	Units
Module size	64.0 ± 0.3 (H) × 85.0 ± 0.3 (V) × (3.96) ± TBD (D)	mm
Display area	53.64 (H) × 71.52 (V) [Diagonal display area: 8.9 cm (Type 3.5)]	mm
Number of pixels	240 (H) × 320 (V)	pixel
Dot pitch	0.0745 (H) × 0.2235 (V)	mm
Pixel pitch	0.2235 (H) × 0.2235 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	-
Display colors	262,144	color
Weight	(37) (Typ.)	g

8. ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Units	Remarks
Supply voltage	VCC	-0.3 to +4.0	V	Ta = 25 °C
	VDD	-0.3 to +6.0	V	Ta = 25 °C
	VGON	-0.3 to +44.0		
	VGOFF	VGON - 44.0 to +0.3		
Logic input voltage	VI	-0.3 to VCC+0.3	V	Logic signals
γ control voltage	V0 to V4	-0.3 to VDD+0.3	V	-
(Back light) Reverse voltage	VR	≤ 15	V	Ta = 25 °C Above value are applied to V1,V2
Power Dissipation	PD	≤ 360	mW	
Storage temperature	Tst	-20 to +70	°C	-
Operating temperature	Top1	0 to +50		Module surface Note: 1
Relative humidity (RH) Note 2		≤ 95	%	Ta ≤ 40°C
		≤ 85		40°C < Ta ≤ 50°C
Absolute humidity Note 2		Absolute humidity shall not exceed Ta = 50°C, RH = 85%.	g/m ³	Ta > 50°C
Storage altitude		≤ 13,600	m	-20°C ≤ Ta ≤ 70°C
Operating altitude		≤ 4,850	m	0°C ≤ Ta ≤ 50°C

Note 1: Measure at the display area

Note 2: No dew condensation

9. ELECTRICAL CHARACTERISTICS**(1) Logic/ LCD driving**

(Ta = 25°C)

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Logic supply voltage	VCC	2.6	3.0	3.6	V	-
H driver supply voltage	VDD	4.75	5.0	5.25	V	-
V driver(+) supply voltage	VGON	14.0	15.0	16.0	V	-
V driver(-) supply voltage	VGOFF	-16.0	-15.0	-14.0	V	-
Logic input high voltage	VIH	0.7×VCC	-	VCC	V	Logic signal
Logic input low voltage	VIL	0	-	0.3×VCC	V	
COM voltage input range	COM	VDD	-	-	Vp-p	-
COM center voltage	COM/C	TBD	TBD	TBD	V	At VDD=5.00V Note 1
VCC supply current	ICC	-	(0.2)	TBD	mA	At VCC= 3.0 V Not include the controller
VDD supply current	IDD	-	(3.5)	TBD	mA	At VDD= 5.00 V
VGON supply current	IGON	-	(0.06)	TBD	mA	At VGON=15.0 V
VGOFF supply current.	IGOFF	-	(0.06)	TBD	mA	At VGOFF= -15.0 V

Note 1: An optimal value for COM/C is in the range of 1.5 to 2.5.

(2) Back light

(Ta = 25°C)

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Forward Current	IL	-	18	20	mA	-
Forward Voltage	VL	8.8	10.6	11.9	V	At IL=18mA

Remark : Above value are applied to V1,V2 each.

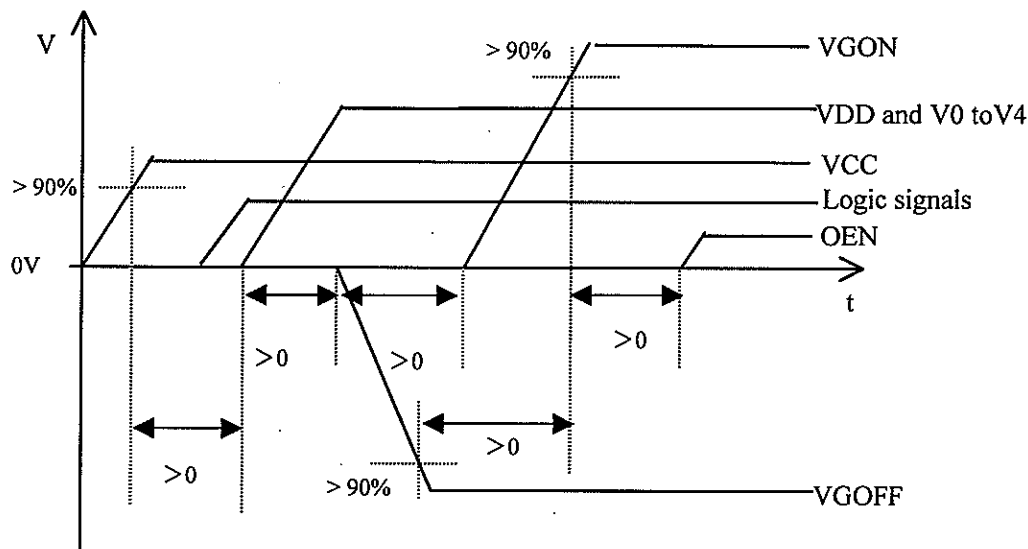
(3) Touch panel

(Ta =

25°C)

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Touch panel input voltage	Vtp	-	-	5.5	V	-
Resistor between terminals(XL-XR)	Rx	(300)	-	(900)	Ohm	-
Resistor between terminals(YU-YD)	Ry	(350)	-	(950)	Ohm	-
Line linearity (X direction)	Xlin	-	-	1.5	%	-
Line linearity (Y direction)	Ylin	-	-	1.5	%	-
Insulation resistance	Rins	20	-	-	Mohm	At DC 25 V
Capacitance	Ctp	-	-	100	nF	-
Chattering	Chat	-	-	10	ms	-
Operation starting force	Ost	10	-	80	g	-

10. SUPPLY VOLTAGE SEQUENCE



Remark 1: Supply voltage sequence must be kept according to the above timings. And when it is turned off, the sequence must be reversed.

Remark 2: The "OEN" signal of the controller should be "H" after VGON.

Remark 3: All signals should not be interrupted during the operation. Even if the signals recover, LCD module may not be operated correctly. In this case, reset the sequence again.

11. INTERFACE PIN CONNECTIONS

(1) Interface connector for signals and power

CNI

Adaptable socket: TBD

Supplier: TBD

Pin No.	Symbols	Functions	Pin No.	Symbols	Functions
1	GND	Ground	24	D24	Blue data
2	COM	Signal for common electrode	25	D25	Blue data (MSB)
3	N.C.	Non-connection	26	D10	Green data (LSB)
4	V0	Gamma control (Non-connection for internal gamma setting)	27	D11	Green data
5	V1		28	D12	Green data
6	V2		29	D13	Green data
7	V3		30	D14	Green data
8	V4		31	D15	Green data (MSB)
9	GAM	Gamma selection switch	32	D00	Red data (LSB)
10	VCOM	Driver output signal	33	D01	Red data
11	N.C.	Non-connection	34	D02	Red data
12	INV	Data reversal signal	35	D03	Red data
13	POL	Polarity reversal signal	36	D04	Red data
14	STB	H driver latch signal	37	D05	Red data (MSB)
15	AP	H driver inhibition signal	38	GND	Ground
16	VCC	Logic voltage	39	VDD	H driver voltage
17	HCK	H driver shift clock	40	VCK	V driver shift clock
18	HSP	H driver start pulse	41	VGOFF	V driver OFF voltage
19	GND	Ground	42	VOE	V driver output enable ("L" output)
20	D20	Blue data (LSB)	43	VGON	V driver ON voltage
21	D21	Blue data	44	VSP	V driver start pulse
22	D22	Blue data	45	GND	Ground
23	D23	Blue data			

Description of terminals

Terminals	Description
COM	This is the Common voltage. The voltage needs to be adjusted. The details are explained the above.
V0 to V4	Provide the gamma setting voltages. Maintain the following voltage relationships. $VSS \leq V4 \leq V3 \leq V2 \leq V1 \leq V0 \leq VDD$
GAM	In cases where the gamma voltages are supplied from outside, GAM needs to be set "H". Otherwise, GAM is "L" or "Open" for internal gamma setting.
VCOM	Output of VDD voltage at the falling edge of STB reversing the signal of POL.
INV	Invert input data signal. Synchronize with the shift clock. INV = L: Normal input INV = H: Invert input data
POL	This pin inverts the output polarity. The polarity inversion signal data is captured at the rising edge of STB. The gamma-resistor is switched in accordance with the positive/negative polarity. POL = H: Positive polarity POL = L: Negative polarity

To be continued

Continued

Terminals	Description
STB	A timing signal that latches the contents of the data register. When an H level is read at the rising edge of CLK, the contents of the data register are latched and transferred to the D/A converter, and analog voltage corresponding to the display data is output. Also, because the internal operation via CLK continues even after the STB latch, do not stop CLK. The contents of the shift register are cleared at the rising edge of STB.
AP	This pin turns on/off the BIAS circuit and turns on the output SW and amplifier. When AP is H, the amplifier is set and the LCD is driving. The amplifier output and output SW are turned on at the rising edge of AP, starting the LCD drive. Note that the output SW is turned off at the rising edge of STB and the output becomes Hi-Z.
HCK	This pin is the shift clock input of the column shift register. Display data is captured into the data register at the rising edge.
HSP	Fetching of display data starts when H is read at the rising edge of CLK.
VCK	This pin is the shift clock input of the gate shift register. The start pulse is captured at the rising edge of clock and output the pulse at the falling edge.
VOE	This pin controls the output of the gate drivers. Output can be controlled regardless of VSP and VCK.
VSP	This pin synchronizes with the frame and the gate driver.

(2) Interface connector for back light

CN2

Adaptable socket: TBD (Supplier: TBD)

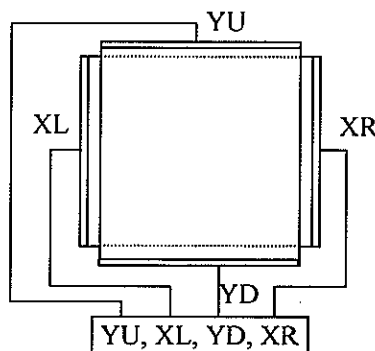
Pin No.	Symbols	Functions
1	(GND)	Ground (left cathode)
2	(V1)	LED 1 Voltage (left anode)
3	(GND)	Ground (right cathode)
4	(V2)	LED 2 Voltage (right anode)

(3) Interface connector for touch panel

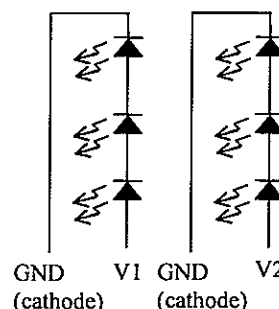
CN3

Adaptable plug: TBD (Supplier: TBD)

Pin No.	Symbols	Functions
1	(YU)	Vertical terminal (Up side)
2	(XL)	Horizontal terminal (left side)
3	(YD)	Vertical terminal (Down side)
4	(XR)	Horizontal terminal (Right side)



Circuits of touch panel



Circuits of back light

Remark : Do not fold FPC (Flexible Printed Circuit) sharply, otherwise, pattern disconnection may be caused.
 In case of folding it, the minimum curvature (R) should be more than 1.0mm.

12. DISPLAY COLORS vs. DISPLAY POSITIONS

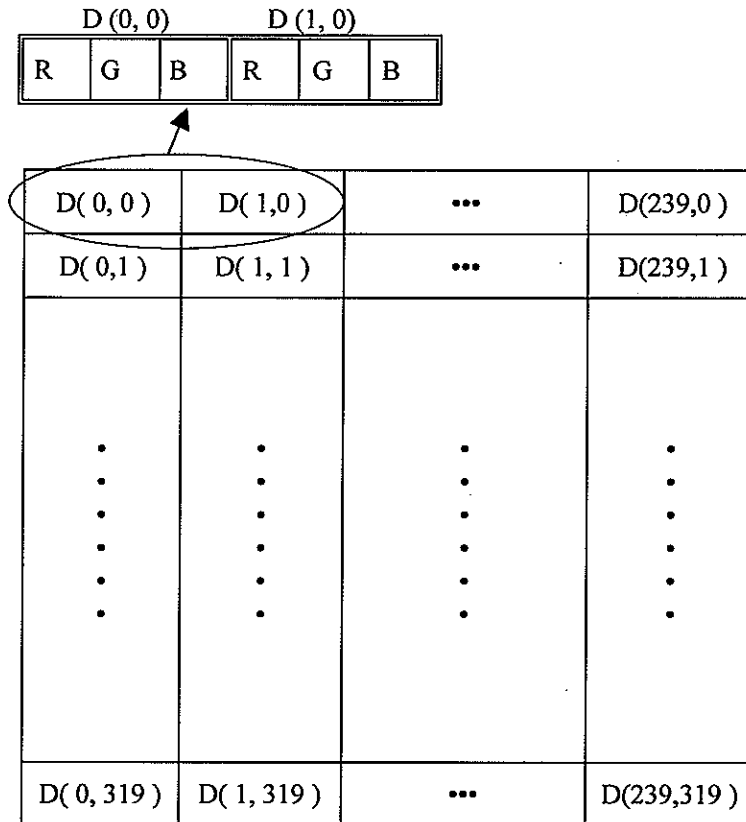
(1) Display colors

Display colors		Data signal(0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	↑																		
	↓																		
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Red	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	↑																		
	↓																		
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
Green	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	
Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	↑																		
	↓																		
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Remark: Colors are developed in combination with 6-bit signals (64 steps in grayscale) of each primary red, green, and blue color.

This process can result in up to 262,144 (64 × 64 × 64) colors.

(2) Display positions of input data



13.INPUT SIGNAL TIMINGS

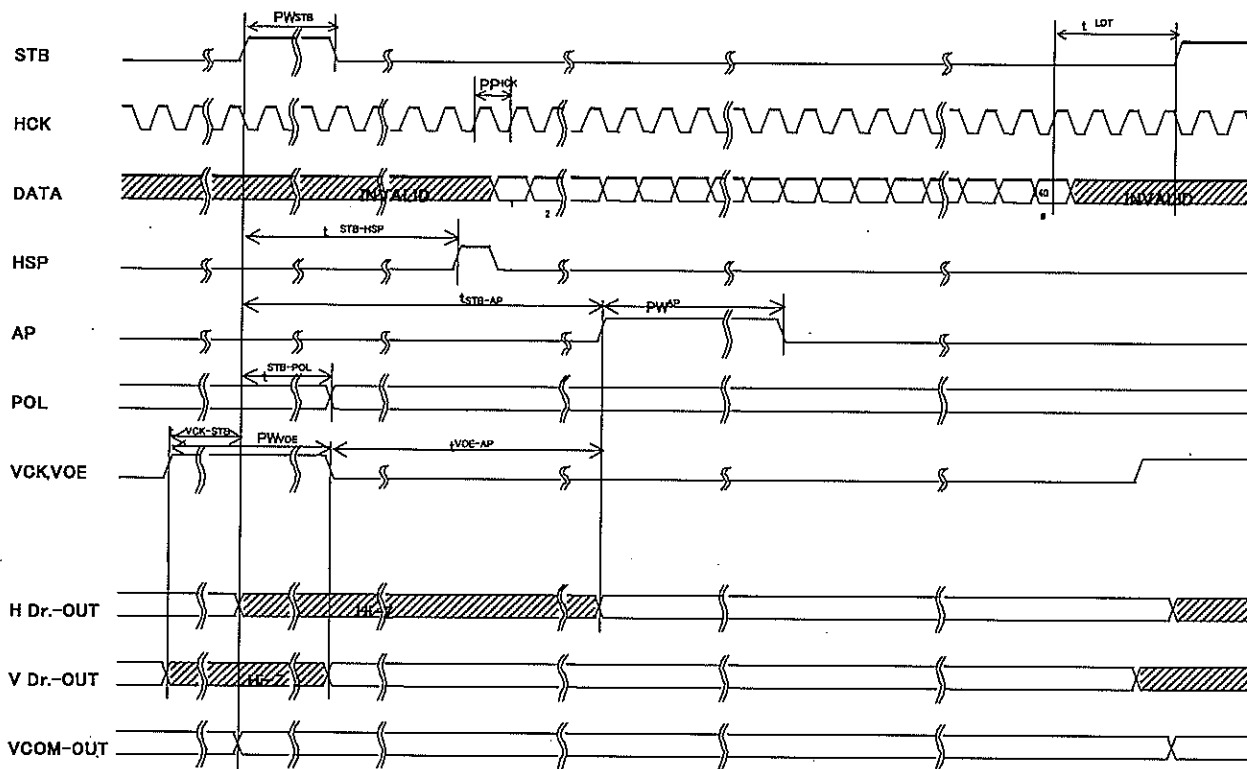
(1)Input signal specifications for LCD controller (Ta=25°C、VCC=3.0V、VDD=5.00V)

Timing characteristic

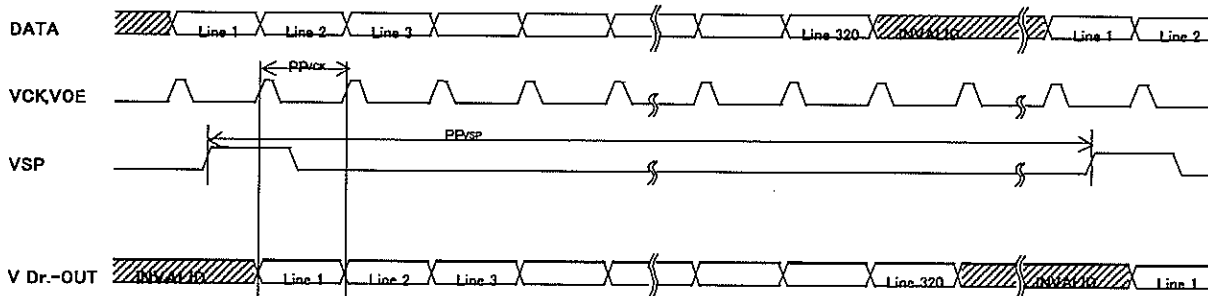
Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Clock frequency	PPHCK	5.4	5.74	7.2	MHz	-
Last data timing	tLDT	2	-	-	CLK	-
STB frequency	PPSTB	16.5	19.9	20.0	kHz	-
STB pulse width	PWSTB	550	-	-	ns	-
STB-HSP time	tSTB-HSP	4	-	-	CLK	-
STB-AP time	tSTB-AP	5	-	-	μs	-
AP pulse width	PWAP	15	-	-	μs	-
VOE-AP time	tVOE-AP	0	10	-	μs	-
STB-POL time	tSTB-POL	40	-	-	ns	-
VCK-STB time	tVCK-STB	1	3	-	μs	-
VSP frequency	PPVSP	50	60	65	Hz	-
Clock frequency	PPVCK	16.5	-	20	kHz	-

Remark: All parameters should be kept within the specified range.

Horizontal timing chart

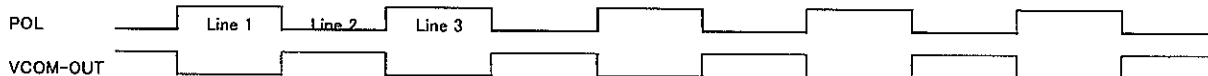


Vertical timing chart



Polarity of signal "POL"

Frame N



Frame N+1



14. OPTICAL CHARACTERISTICS

< Back light turning off >

Note 1

Parameters	Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks
Contrast ratio	CR	-	TBD	(10:1)	-	-	Note 2,3
Reflection ratio	RE	-	TBD	(7)	-	%	Note 3

Reference data

Note 1

Parameter	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks	
Chromaticity coordinates	W	White (x, y)	-	TBD, TBD	-	-	Note 3	
Color gamut	C	-	TBD	TBD	TBD	%	Remark	
Response time	Ton	White to black	90%→ 10%	-	TBD	TBD	ms	Note 6
	Toff	Black to white	10%→ 90%	-	TBD	TBD		

Remark : Against NTSC color space

< Back light turning on >

Note 1

Parameters	Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks
Contrast ratio	CR	IL= 18mA	TBD	TBD	-	-	Note 2,4
Luminance	Lu	IL= 18mA	TBD	TBD	-	cd/m ²	Note 4
Luminance uniformity	-	Maximum luminance: 100%	TBD	(70)	-	%	Note 5

Reference data

Note 1

Parameter	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks	
Chromaticity coordinates	W	White (x, y)	-	TBD, TBD	-	-	Note 4	
Color gamut	C	IL= 18mA	TBD	TBD	TBD	%	Remark	
Response time	Ton	White to black	90%→ 10%	-	TBD	TBD	ms	Note 6
	Toff	Black to white	10%→ 90%	-	TBD	TBD		

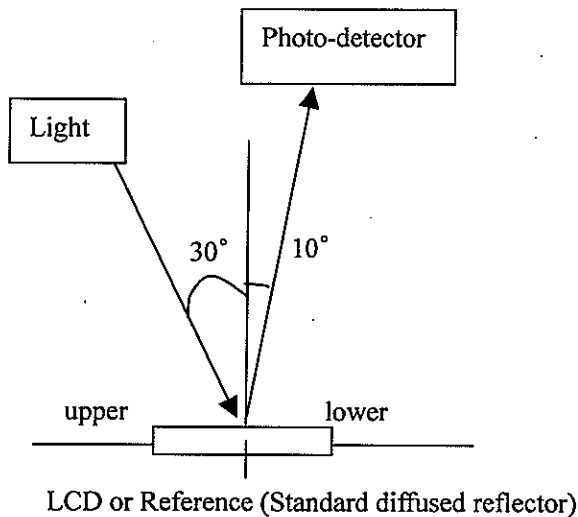
Remark : Against NTSC color space

Note 1 : Ta = 25°C, VCC=3.0V, VDD=5.0V, Include back light and touch panel

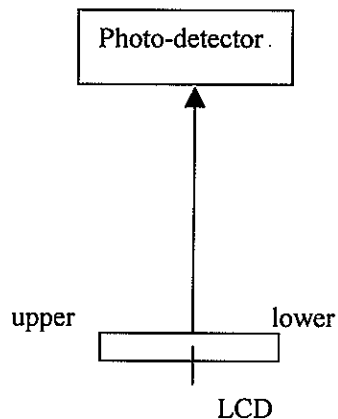
Note 2 : The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Reflection ratio (Luminance) with all pixels in "white"}}{\text{Reflection ratio (Luminance) with all pixels in "black"}}$$

Note 3: Contrast ratio and reflection ratio are measured as follows.



Note 4: Contrast ratio, Chromaticity coordinates and Luminance are measured as follows.

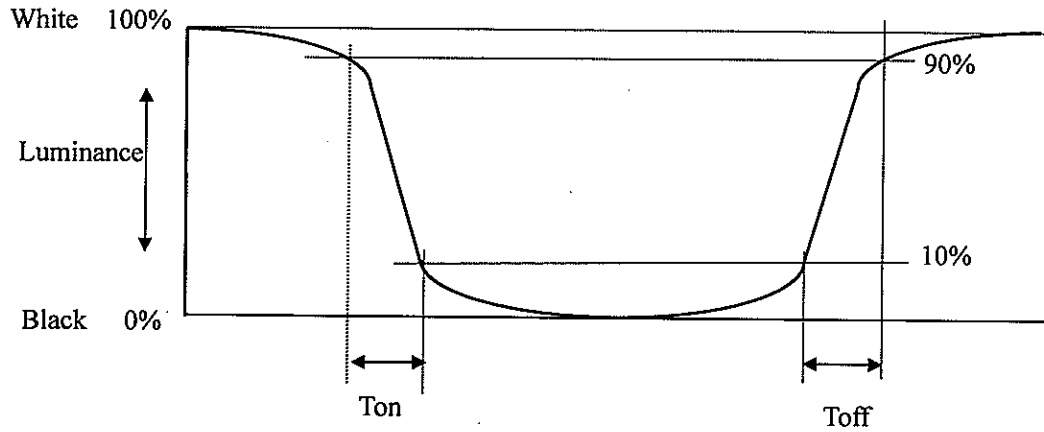


Note 5: Note6: Luminance uniformity is calculated by using the following formula.

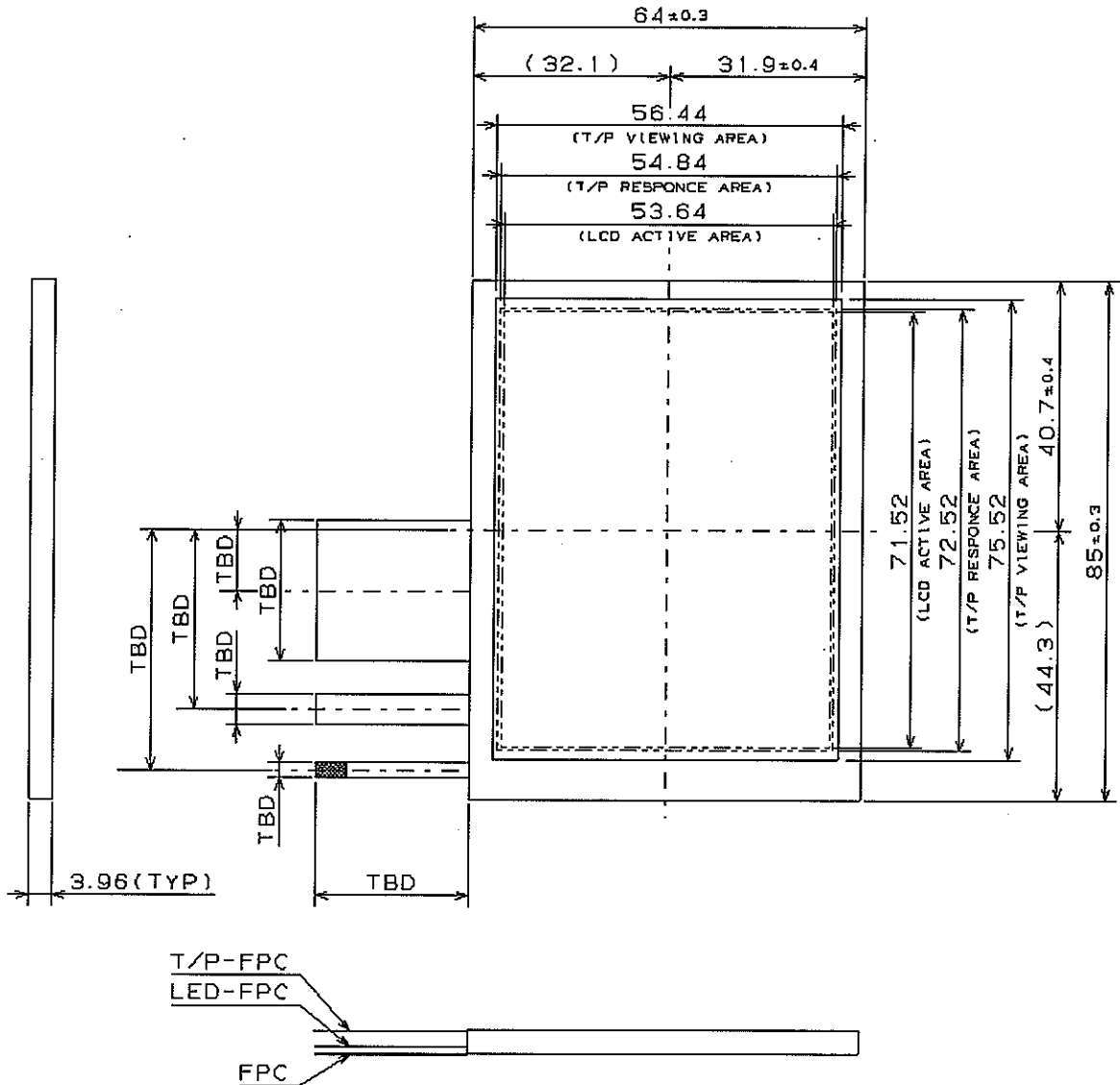
$$\text{Luminance uniformity (\%)} = \frac{\text{Minimum luminance}}{\text{Maximum luminance}} \times 100$$




Note 6: Definitions of response time is as follows.

Photo-detector output signal is measured when the luminance changes "white" to "black" or "black" to "white".



15. OUTLINE DRAWINGS



Revision History				DOD-M-1252		19/19
Rev.	Prepared Date	Revision contents	Approved	Checked	Prepared	Issued Date
1	Nov.28 2002	DOD-M-1252	 H. Yamaguchi i	 T. Shinohara	 Y. Ito	-